Neelkanth Institute of Technology Meerut

Department of Electronics and Communication

VLSI DESIGN ASSIGNMENT 1

The goal of this assignment is to understand the MOSFET behavior and extract few model parameters that are useful in the coming (design) assignments.

1 Process technology details

1. Use the digital MOSFETs in UMC 180nm technology.
2. Core voltage (V_{DD}) for this technology is 1.8 V.
3. Model file (contains both nmos and pmos transistor) is located at
   /tools/public/asiclib/umc/L180/process/UMC_MM_RF_CO1/Models/MM180_Model_1.5_P3/Spectre/MM180_REG18_V124.mdl.scs
4. You might need to include the following library file (in-fact this alone is sufficient. Why?).
   /tools/public/asiclib/umc/L180/process/UMC_MM_RF_CO1/Models/MM180_Model_1.5_P3/Spectre/MM180_REG18_V124.lib.scs
5. Use the section "tt" while including the above library file. To know what these sections in the library file mean, please read sec. 3.4 of [1]
6. Discussing with your friends is highly encouraged (but not copying).

2 Operating regions and their transition

In general, we use minimum length devices for the design of digital circuits (Why? And this is not true for analog circuits in general. Any guesses, why not?). In these minimum length devices all the three regions namely exponential (subthreshold), quadratic and linear (velocity saturation), will present in the I_D vs. V_{GS} characteristics. These regions are clearly visible in the $ln(I_D)$ vs. V_{GS} characteristics. Please refer page no. 88-100 of [1].

1. For minimum length and width of NMOS, draw the $log_{10}(I_D)$ vs. V_{GS} (Please note that we have taken log_{10} rather than ln) characteristics at $V_{DS} = 0.5$, 1, 1.5, 1.8 V.
2. Identify the boundary point, ($V_{Gst} \sim V_T$, I_{Dst}), between the exponential and quadratic regions (Just mark the approximate point on graph and note it down on a paper/file. I_{Dst} need some re-computation). Also note down the slope of the curve in the exponential region and calculate the $n-$factor. (Plot should look like that in Figure 3-22 of [1])
3. Plot V_T vs. V_{DS} from the above results. (You can use excel/matlab/any other tool. Plot should look like that in Figure 3-36 (b) of [1])
4. To identify the boundary between quadratic and linear regions, plot the $\frac{\partial}{\partial V_{GS}}(I_D)$ vs. V_{GS} and note down the boundary point (V_{Gvt}, I_{Dvt}).
5. Repeat the exercise for PMOS as well.
6. Tabulate the voltage ranges, for different regions of operations, for NMOS and PMOS.

3 Develop a model for manual analysis

Plot the I_D vs. V_{DS} characteristics for $V_{GS} = 2V_T$, $3V_T$, V_{DD}. Develop a **unified model** as explained

in page no. 101-103 of [1]. You can read/cross-check some of the parameters from the model file (Deliverables include: an overlap plot like Figure 3.25 (again, you can use any tool like excel/matlab) and a table like 3.2 of [1] for each of NMOS and PMOS).

4 Modeling of AC-resistance

1. Using the Model you have developed previously and equation 3.43 of [1], calculate the R_{eq1}.
2. Keeping $V_{GS} = V_{DD}$, plot $1/\frac{\partial}{\partial V_{DS}}(I_D)$ vs. V_{DS} for $V_{DD} = 1,\ 1.5,\ 1.8$. Now compute avg.$(R_{eq2} = 1/(\frac{\partial}{\partial V_{DS}}(I_D)))$ for $V_{DS} = V_{DD}/2$ to V_{DD}.
3. Develop a table similar to the one in table 3-3 of [1] but include both R_{eq1} and R_{eq2}.
4. Do it for PMOS as well.

5 Extraction of different capacitances

1. Read the following parameters from the model file for "tt" process. ϵ_{ox}, t_{ox} and $c_{gso} = c_{gdo}$. Using equation 3.44 and 3.46, table 3.4 of [1] compute C_{GS} and C_{GD} (Need not to compute other capacitances).
2. Plot the $C_G - V_{GS}$ characteristics of both NMOS and PMOS. Please look at the example 3.9 for the test circuit and the method.
3. Plot the $C_D - V_{DS}$ characteristics of both NMOS and PMOS. You need to adapt the test-circuit suitably.
4. Compare your hand calculated results and simulated results in a table. Give few comments/reasons for any deviations.

6 Deadlines-Deliverables

6.1 Deliverables

A document (.pdf format only) with all your plots, analyses, tables and calculations. Please use extra font size for labels and wider lines for plots (so that they are readable even when you reduce the figure size in your pdf). Your document should contain your name and entry no. Evaluation is solely based on this document.

6.2 Method of delivery

Please mail your documentation and scripts/netlists to [redacted]

6.3 Deadline

11.59 PM on [redacted]

References

[1] Jan. M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, *Digital Integrated Circuits - A Design Perspective*, chap.3, 2nd ed. Delhi, India: Pearson Prentice Hall, 2003.

Additional useful notes from other books

1. The transition voltage between exponential and quadratic characteristics (which we have assumed equal to V_T in the above exercise) is $V_{GS} = V_T + 2n(KT/q)$ or $(V_{GS} - V_T) = 2n(KT/q) \sim 70mV$ and is independent of L. Therefore in any technology, if you can choose $(V_{GS} - V_T) > 100mV$ you will be safely out of exponential region.
2. Similarly the transition voltage between quadratic and linear regions is $(V_{GS} - V_T) \sim 5L$ (L in μm). And for any lower technologies we can now estimate the boundary of velocity saturation. Is it matching with your answer?
3. $\frac{\partial}{\partial V_{GS}}(I_D)$ is called the trans conductance of the transistor, denoted by g_m. From the plot you have drawn, you could observe that there exists an upper bound on the maximum achievable g_m. This occurs in the velocity saturation (i.e., our linear region) and its value is $WC_{ox}\vartheta_{sat}$. Check whether it is true or not. (For this technology, $(\vartheta_{sat})_n \sim 7.158X10^4$ m/s and $(\vartheta_{sat})_p \sim 5.34X10^4$ m/s)